WHAT IS CLAIMED IS:

1. A method of fabricating a transistor, the method comprising:

providing a workpiece;

growing a stressed semiconductor layer over the workpiece;

growing a first layer of silicon and carbon over the stressed semiconductor layer;

depositing a gate dielectric material over the layer of silicon and carbon;

depositing a gate material over the gate dielectric material;

patterning the gate material and gate dielectric material to form a gate and a gate dielectric disposed over the layer of silicon and carbon; and

forming a source region and a drain region in the layer of silicon and carbon and stressed semiconductor layer, wherein the source region, drain region, gate, and gate dielectric comprise a transistor.

2. The method according to Claim 1, wherein growing the layer of silicon and carbon comprises epitaxially growing a layer of about 90 to 99.5% silicon and about 0.5 to 10 % carbon having a thickness of about a few tens of Å to about 5 μm.

3. The method according to Claim 1, wherein growing the stressed semiconductor layer comprises epitaxially growing a second layer of silicon and carbon, a layer of silicon and germanium, or a layer of silicon, carbon and germanium, and wherein growing the stressed semiconductor layer comprises growing a material having a thickness of about 100 Å to about 5 μm.

4. The method according to Claim 1, wherein depositing the gate dielectric material comprises depositing a high k dielectric material or an oxide, and wherein depositing the gate material comprises depositing a semiconductor material or a metal.

5. The method according to Claim 1, further comprising depositing a thin semiconductor material over the first layer of silicon and carbon, before depositing the gate dielectric material.

6. The method according to Claim 5, wherein depositing the thin semiconductor material comprises depositing about 100 Å or less of Si, Ge, SiGe, a bilayer of Si/SiGe, or a bilayer of Ge/SiGe.

7. The method according to Claim 1, further comprising forming isolation regions in the workpiece, before or after growing the stressed semiconductor layer over the workpiece and growing a first layer of silicon and carbon over the workpiece, and further comprising forming spacers over sidewalls of the gate and gate dielectric.

8. The method according to Claim 1, wherein providing the workpiece comprises providing a silicon-on-insulator (SOI) wafer.

9. A method of fabricating a transistor, the method comprising:

providing a workpiece;

growing a first layer of silicon and carbon over the workpiece;

depositing a gate dielectric material over the layer of silicon and carbon, the gate dielectric comprising a high dielectric constant (k) material;

depositing a gate material over the gate dielectric material, the gate material comprising a metal;

patterning the gate material and gate dielectric material to form a gate and a gate dielectric disposed over the layer of silicon and carbon; and

forming a source region and a drain region in at least the layer of silicon and carbon, wherein the source region, drain region, gate, and gate dielectric comprise a transistor.

10. The method according to Claim 9, wherein growing the layer of silicon and carbon comprises epitaxially growing a layer of about 90 to 99.5% silicon and about 0.5 to 10 % carbon having a thickness of about a few tens of Å to about 5 μm.

11. The method according to Claim 9, further comprising growing a stressed semiconductor layer over the workpiece, before growing the first layer of silicon and carbon over the workpiece, wherein forming the source region and the drain region comprises forming the source region and the drain region in the stressed semiconductor layer.

12. The method according to Claim 11, wherein growing the stressed semiconductor layer comprises epitaxially growing a second layer of silicon and carbon, a layer of silicon and germanium, or a layer of silicon, carbon and germanium, and wherein growing the stressed semiconductor layer comprises growing a material having a thickness of about 100 Å to 5 μm.

13. The method according to Claim 9, further comprising depositing a thin semiconductor material over the first layer of silicon and carbon, before depositing the gate dielectric material.

14. The method according to Claim 13, wherein depositing the thin semiconductor material comprises depositing about 100 Å or less of Si, Ge, SiGe, a bilayer of Si/SiGe, or a bilayer of Ge/SiGe.

15. The method according to Claim 9, further comprising forming isolation regions in the workpiece, before or after growing the stressed semiconductor layer over the workpiece and growing a first layer of silicon and carbon over the workpiece, and further comprising forming spacers over sidewalls of the gate and gate dielectric.

16. The method according to Claim 9, wherein providing the workpiece comprises providing a silicon-on-insulator (SOI) wafer.

17. A transistor, comprising:

a workpiece;

a stressed semiconductor layer disposed over the workpiece;

a first layer of silicon and carbon disposed over the stressed semiconductor layer;

a gate dielectric disposed over the layer of silicon and carbon;

a gate disposed over the gate dielectric; and

a source region and a drain region formed in the layer of silicon and carbon and stressed semiconductor layer, wherein the source region, drain region, gate, and gate dielectric comprise a transistor.

18. The transistor according to Claim 17, wherein the layer of silicon and carbon comprises an epitaxially grown layer comprising about 90 to 99.5% silicon and about 0.5 to 10 % carbon having a thickness of about a few tens of Å to about 5 μm.

19. The transistor according to Claim 17, wherein the stressed semiconductor layer comprises an epitaxially grown second layer of silicon and carbon, a layer of silicon and germanium, or a layer of silicon, carbon and germanium, and wherein the stressed semiconductor layer comprises a thickness of about 100 Å to 5 μm.

20. The transistor according to Claim 17, wherein the gate dielectric comprises a high k dielectric material or an oxide, and wherein the gate comprises a semiconductor material or a metal.

21. The transistor according to Claim 17, further comprising a thin semiconductor material disposed over the first layer of silicon and carbon.

22. The transistor according to Claim 21, wherein the thin semiconductor material comprises about 100 Å or less of Si, Ge, SiGe, a bilayer of Si/SiGe, or a bilayer of Ge/SiGe.

23. The transistor according to Claim 21, further comprising isolation regions disposed in the workpiece, and further comprising spacers formed over sidewalls of the gate and gate dielectric.

24. The transistor according to Claim 21, wherein the workpiece comprises a silicon-on-insulator (SOI) wafer.

25. A transistor, comprising:

a workpiece;

a first layer of silicon and carbon disposed over the workpiece;

a gate dielectric disposed over the layer of silicon and carbon, the gate dielectric comprising a high dielectric constant (k) material;

a gate disposed over the gate dielectric, the gate comprising metal; and

a source region and a drain region formed in at least the layer of silicon and carbon, wherein the source region, drain region, gate, and gate dielectric comprise a transistor.

26. The transistor according to Claim 25, wherein the layer of silicon and carbon comprises an epitaxially grown layer comprising about 90 to 99.5% silicon and about 0.5 to 10 % carbon having a thickness of about a few tens of Å to about 5 μm.

27. The transistor according to Claim 25, further comprising a stressed semiconductor layer formed over the workpiece beneath the first layer of silicon and carbon, wherein the source region and the drain are also formed in the stressed semiconductor layer.

28. The transistor according to Claim 27, wherein the stressed semiconductor layer comprises a second layer of silicon and carbon, a layer of silicon and germanium, or a layer of silicon, carbon and germanium, and wherein the stressed semiconductor layer comprises a material having a thickness of about 100 Å to 5 μm.

29. The transistor according to Claim 25, further comprising a thin semiconductor material disposed over the first layer of silicon and carbon, beneath the gate dielectric material.

30. The transistor according to Claim 29, wherein the thin semiconductor material comprises about 100 Å or less of Si, Ge, SiGe, a bilayer of Si/SiGe, or a bilayer of Ge/SiGe.

31. The transistor according to Claim 25, further comprising isolation regions formed in the workpiece, and further comprising spacers formed over sidewalls of the gate and gate dielectric.

32. The transistor according to Claim 25, wherein the workpiece comprises a silicon-on-insulator (SOI) wafer.